Abstract

First and second chips each having a transistor are provided. The first chips are arranged along a first axis on a first metallic body in side-by-side and interspaced manner. The second chips are arranged parallel to the first axis on a second metallic body in a side-by-side and interspaced manner. The second chips are arranged perpendicular to the first axis opposite an area of the first body and are each connected to the opposite area via at least one bonding connection. The first chips, with regard to the third axis, are arranged opposite an area of the second body, which is located between adjacent second chips. A third metallic body is arranged on the second body and comprises projections each of which being arranged on one of the areas of the second body. The first chips are each connected to the opposite projection via at least one bonding connection.